The opinion in support of the decision being entered today was not written for publication and is not binding precedent of the Board.

Paper No. 18

UNITED STATES PATENT AND TRADEMARK OFFICE

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BEFORE THE BOARD OF PATENT APPEALS
AND INTERFERENCES

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Ex parte HAROLD L. MASSIE, EDWARD L. PAYTON,
and ROBERT D. WICKERSHAM

_____

Appeal No. 1999-1992
Application No. 08/848,842

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ON BRIEF

_____

Before LALL, LEVY, and BLANKENSHIP, Administrative Patent Judges.

LALL, Administrative Patent Judge.

DECISION ON APPEAL

This is a decision on appeal under 35 U.S.C. § 134 from the final rejection[1] of claims 1-10, 12-19, and 22. Claims 11, 20, and 21 have been canceled.

The invention is directed to a Direct-Current (DC) to Direct-Current (DC) converters. They are typically employed to convert from one DC voltage signal level to another DC voltage signal level. One situation that is frequently an issue with such converters occurs when a sizable load is applied to the converter. A relatively sudden increase in load may be approximated as a step function and, as is well-known, typically results in a transient voltage signal in the circuitry to which the step function is applied. Such transients are undesirable because one of the functions of a DC-to-DC converter is to maintain an output voltage signal level within a particular voltage signal window or a set of voltage signal boundaries to ensure, for example, that the operation of the circuitry being powered by the DC-to-DC converter is not substantially affected by the sudden increase

[1] An amendment after final rejection was filed as Paper No. 11, the examiner approved its entry, see Paper No. 12. However, we note that the amendment has not been physically entered into the record. We refer this matter to the examiner, to ensure entry of the amendment.

in load. Conventionally, the DC-to-DC converters address this situation by employing bulk capacitance. Unfortunately, the use of bulk capacitance has several disadvantages. Therefore, it would be desirable if a technique or a method were available to reduce the amount of capacitance employed with a DC-to-DC converter while still providing the capability of the DC-to-DC converter to maintain the output voltage signal level within the desired voltage signal window or voltage signal level bounds, even when a sizable or significant load is applied. One embodiment of the invention comprises a circuit configuration to adjust the output voltage signal level of the DC-to-DC converter as a function of the output current signal. For this embodiment of a DC-to-DC converter, higher current signal levels lower the output voltage signal level by a proportional amount. This adjustment of output voltage signal level provides increased voltage margin to respond to load changes producing output current signal changes. In this way, the circuitry of the invention effectively adjusts the set point of the output voltage signal level in response to voltage signal transients, such as from an increase in load. The set point refers to a voltage signal level about which the

circuit tends to operate in equilibrium. By having the capability to adjust the set point of the output voltage signal level, the output voltage signal may be set within a predetermined window at a voltage signal level providing additional voltage margin to respond to an increase in load, if one should occur. With this additional voltage margin, less capacitance may be employed because the additional voltage margin may be employed to at least partially offset the transient voltage signal. A further understanding of the invention can be obtained by the following claim.

1. A DC-to-DC converter circuit comprising: a circuit configuration to modify the set point of the output voltage signal of the DC-to-DC converter circuit in response to a transient signal by an amount related, at least in part, to the magnitude of the transient signal.

The examiner relies on the following references[2]:

Davis et al. (Davis)	4,355,277	Oct. 19, 1982
Farwell	5,670,865	Sep. 23, 1997 (filed Aug. 29, 1996)
Kolluri et al. (Kolluri)	5,721,483	Feb. 24, 1998

[2] The examiner lists two other patents, U.S. patent No. 4,618,812 to Kawakami and U.S. patent No. 4,161,023 to Goffeau as part of the prior art of record on page 3 of the examiner's answer. However, these two patents do not form part of the rejection before us. Therefore, we do not consider Kawakami and Goffeau in our deliberations for this decision.

(filed Sep. 15, 1994)

Claims 1-4, 7-9, 12-19, and 22 stand rejected under 35 U.S.C. § 102 as being anticipated by Farwell. Claims 5 and 10 stand rejected under 35 U.S.C. § 103 as being unpatentable over Farwell in view of Kolluri, while claim 6 stands rejected over Farwell in view of Davis.

Rather than repeat the positions and the arguments of appellants and the examiner, we make reference to the briefs[3] and the answer for their respective positions.

OPINION

We have considered the rejections advanced by the examiner. We have, likewise, reviewed appellants' arguments against the rejections as set forth in the briefs.

We reverse.

The examiner rejects all the independent claims, namely, claims 1, 8, 13 and 17 as being anticipated under 35 U.S.C. § 102 by Farwell. For the explanation of the rejection, the examiner merely makes a reference to the abstract and Figure 1 of Farwell. A prior art reference anticipates the subject of

[3] A reply brief was filed as Paper No. 16 and was entered into the record without any further response from the examiner, see Paper No. 17.

a claim when the reference discloses every feature of the claimed invention, either explicitly or inherently, See Hazani v. Int'l Trade Comm'n, 126 F.3d 1473, 1477, 44 USPQ2d 1358, 1361 (Fed.
Cir. 1997) and RCA Corp. v. Applied Digital Data Sys., Inc., 730 F.2d 1440, 1444, 221 USPQ 385, 388 (Fed. Cir. 1984).

On page 9 of the brief, appellants argue that "the Farwell patent does not relate at all to modifying the set point of the output voltage signal, as claimed . . . ." The examiner's response, answer at page 6 is that "figure 1 of the Farwell patent, a [sic, is] the transient voltage, clearly labeled as the input to the two differential amplifiers with the voltage set points - ^{a}V and + ^{a}V, connected to the two different differential amplifiers 31 and 32, respectively."

We have studied the Farwell patent and reviewed the examiner's comments regarding Figure 1. We, like appellants, find no disclosure in Farwell where the set point of the output voltage is being adjusted in response to the transients caused by a load on the converter. The set points, - ^{a}V and + ^{a}V, which the examiner calls the claimed "set point" are independent of the output voltage of the converter. They

merely serve as the threshold voltage signals for the operation of amplifiers 31 and 32. Therefore, we cannot sustain the anticipation rejection of claim 1 over Farwell.

With respect to claim 8, appellants point out on page 12 of the brief that "the Farwell patent has nothing to do with cross-conduction as claimed" and furthermore the Farwell patent does not, brief at page 13, show "clamping the control voltages of the switching devices in the manner claimed."

We agree with appellants' position. In Farwell, the output of either amplifier 31 or 32 renders the FET 41 or FET 42 conductive depending upon the value of the transient voltage. Therefore, the input to the converter, VIN, either bypasses the DC-to-DC voltage converter 11 or goes through it. Thus, the output voltage of the two amplifiers do not directly affect each other's operation. But, even if we assume that the examiner's statement on page 7 of the examiner's answer, namely, "[o]nly one switch will be on at a time to prevent cross conduction for a positive transient condition and only the other switch will be on for the negative going transient condition" is correct, we do not see the claimed clamping of the controlled voltage of each of the said switches in a low

state while a control voltage of the other device is in a high state. The examiner likewise does not specifically point out this feature in Farwell. Therefore, we cannot sustain the anticipation rejection of claim 8 by Farwell.

With respect to claim 13, we find that this claim contains the recitation of modifying the set point of the output voltage and adjusting the set point based, at least in part, on the magnitude of the sample voltage signal. As we pointed out earlier in our discussion of claim 1, and as argued by appellants on page 14 of the brief, we do not find Farwell to disclose or suggest the modifying of the set point of the output voltage of the converter. Therefore, we do not sustain the anticipation rejection of claim 13 by Farwell.

With respect to claim 17, it too contains the recited limitation of "clamping the control voltage signal of each of the high-side and low-side devices in a low state while the other switching device is in a high state." Therefore, we do not sustain the anticipation rejection of claim 17 for the rationale for claim 8.

Furthermore, in our analysis for obviousness, we are guided by the general proposition that in an appeal involving

a rejection under 35 U.S.C. § 103, an examiner is under a burden to make out a prima facie case of obviousness. If that burden is met, the burden of going forward then shifts to the applicant to overcome the prima facie case with argument and/or evidence. Obviousness is then determined on the basis of the evidence as a whole and the relative persuasiveness of the arguments. See In re Oetiker, 977 F.2d 1443, 1445, 24 USPQ2d 1443, 1444 (Fed. Cir. 1992); In re Hedges, 783 F.2d 1038, 1039, 228 USPQ 685, 686 (Fed. Cir. 1986); In re Piasecki, 745 F.2d 1468, 1472, 223 USPQ 785, 788 (Fed. Cir. 1984); and In re Rinehart, 531 F.2d 1048, 1052, 189 USPQ 143, 147 (CCPA 1976). We are further guided by the precedent of our reviewing court that the limitations from the disclosure are not to be imported into the claims. In re Lundberg, 244 F.2d 543, 113 USPQ 530 (CCPA 1957); In re Queener, 796 F.2d 461, 230 USPQ 438 (Fed. Cir. 1986). We also note that arguments not made separately for any individual claim or claims are considered waived. See 37 CFR § 1.192(a) and (c). In re Baxter Travenol Labs., 952 F.2d 388, 391, 21 USPQ2d 1281, 1285 (Fed. Cir. 1991) (“It is not the function of that court to examine the claims in greater detail than argued by

an appellant, looking for nonobviousness distinctions over the prior art.");

In re Wiechert, 370 F.2d 927, 936, 152 USPQ 247, 254 (CCPA 1967)("This court has uniformly followed the sound rule that an issue raised below which is not argued in this court, even of it has been properly brought here by reason of appeal is regarded as abandoned and will not be considered. It is our function as a court to decide disputed issues, not to create them.").

The examiner rejects claims 5 and 10 over Farwell and Kolluri, as set forth on page 5 of the examiner's answer. However, claims 5 and 10 respectively claim at least the limitations of the independent claims 1 and 8, and Kolluri does not cure the deficiency noted above regarding the rejection of claims 1 and 8 by Farwell. Therefore, the rejection of claims 5 and 10 over Farwell and Kolluri is not sustainable.

Claim 6 is rejected as being obvious over Farwell and Davis on page 5 of the examiner's answer. Again, we note that claim 6 depends from claim 1 and contains at least the limitations of claim 1. Davis does not cure the deficiency

noted above in the rejection of claim 1 by Farwell. Therefore, we cannot sustain the obviousness rejection of claim 6 over Farwell and Davis.

In summary, we have not sustained the rejections under 35 U.S.C. § 102 of claims 1-4, 7-9, 12-19 and 22 as being anticipated by Farwell. Nor have we sustained any of the rejections under 35 U.S.C. § 103 of claims 5 and 10 over Farwell and Kolluri, and of claim 6 over Farwell and Davis.

The decision of the examiner rejecting claims 1-10, 12-19 and 22 is reversed.

REVERSED

Parshotam S. Lall Administrative Patent Judge	)	
Stuart S. Levy Administrative Patent Judge	)	BOARD OF PATENT APPEALS AND INTERFERENCES
Howard B. Blankenship Administrative Patent Judge	)	

PSL:tdl

Appeal No. 1999-1992
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Blakely, Sokoloff, Taylor and Zafman
Howard Skaist
12400 Wilshire Blvd., 7th Floor
Los Angeles, CA 90025